



KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE

Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506015, TELANGANA, INDIA

కాకతీయ ప్రొद्योगికీ एवं विज्ञान संस्थान, वरंगल - ५०६०१५, तेलंगाना, भारत

కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - ౫౦౬ ౦౧౫ తెలంగాణ, భారతదేశము

(An Autonomous Institute under Kakatiya University, Warangal)

(Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by EKASILA EDUCATION SOCIETY)

website: www.kitsw.ac.in

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Department of Electronics Communication and Instrumentation Engineering

Department Research & Education Centre (DREC)

VLSI



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About DREC:

VLSI (Very Large Scale Integration) Research & Education Centre focused on activities related to the design, development, and education in the field of integrated circuits and systems.

Key aspects of DREC - VLSI:

- Research in VLSI Design
- Education and Training
- Publications and Conferences
- Innovation and Prototyping
- Interdisciplinary Research



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Functions of DREC:

- Developing new architectures and design paradigms to meet the evolving demands of electronic systems.
- Offering courses and training programs to educate students, researchers, and industry professionals in VLSI design.
- Providing hands-on experience with VLSI design tools, simulation techniques, and programming to build practical skills.
- Supervising student projects and internships related to VLSI design.
- Providing a platform for students to gain practical experience and contribute to ongoing research activities.



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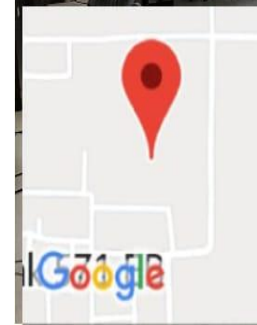
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Major Equipment & Software

S. No.	Equipment Name	Cost
1.	SPARTAN 6 ATLYS Boards	2,00,000.00
2.	Digilent Nexys 4DDR FPGA KITS	1,95,880.00
3.	Desktop Systems	6,44,250.00
4.	MATLAB R2023b	7,60,573.00
5.	Xilinx Vivado Design Suite	2,00,000.00
6.	JAVA & Dev-C++	



DREC-VLSI, Telangana, India
 Block-I-219, Hanumakonda, Telangana 506009,
 India
 Long 79.537546°
 Lat 18.053986°
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Projects / Research carried out in DREC - VLSI

S. No.	Name of the Project / Research carried out in the DREC
1.	Research on Design of 0.8 V, 22 nm DG-FinFET based efficient VLSI multiplexers
2.	Research on A 16 nm finfet circuit with triple function as digital multiplexer, active-high and active-low output decoder for high-performance sram architecture
3.	Research on Design of efficient 22 nm, 20-FinFET full adder for low-power and high-speed arithmetic units
4.	PG Student Project on Simulation and synthesis of UART through FPGA Zedboard for IoT applications



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UG Student Project on Implementation of parallel multiplier based on Booth computing method using FPGA

